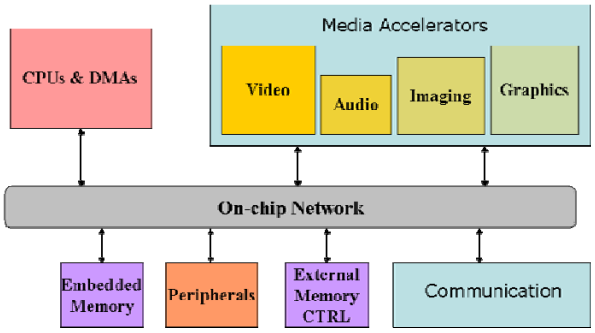
Spidergon STNoC:

The Communication Infrastructure for Multiprocessor Architectures

Marcello Coppola

SoC Today: Size and scalability issues

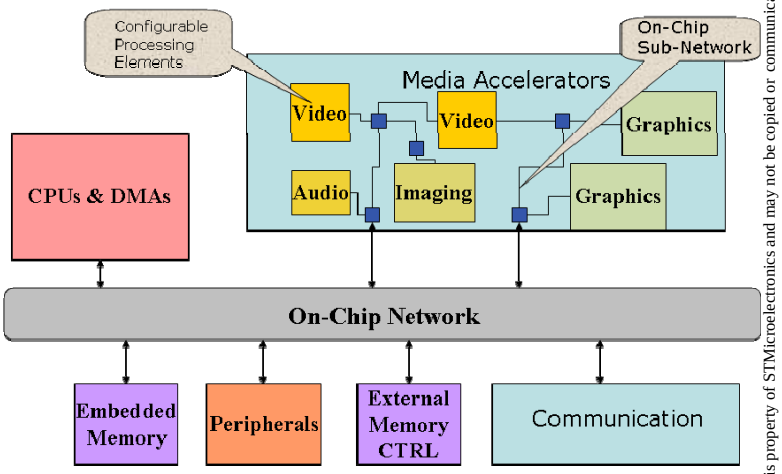
- Current SoC made of specialized subsystem
  - Sized for worst case
  - Not designed to cooperate for future use case
- Heterogeneous and static application software
- Inter IPs communicate through global memory
- Unlikely to support unplanned use case



Highly Inefficient

Programmable SoC: The New Evolution

- Replace heterogeneous dedicated subsystems by specialized configurable (heterogeneous) multi-cores interconnected by an on-chip sub-network
- Overcome variability issues by decoupled power and frequency nodes
  - Dynamic application re-configurability
  - Allows optimal use of computing resources for the given use case

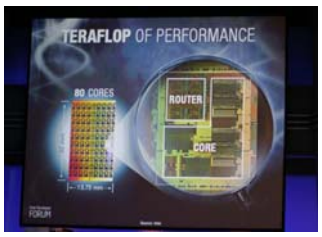


On-chip communication centric platform: our vision

- **Physical-aware interconnect in 45, 32 nm**
  - higher distribution, deeper hierarchy, regularity
  - redundancy & fault tolerance
- **Performance scalability**
  - Higher aggregate bandwidth and concurrency, low latency, power efficiency
  - Advanced communication primitives to enable new programming models
- **Integration platform**
  - Reuse needs, EDA support, productivity
- **Software view of the hardware platform through Services Set**
  - Expose system hardware to system software

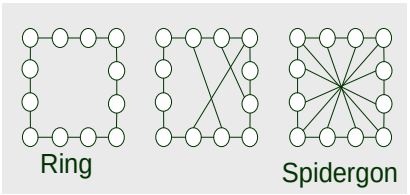
Spidergon STNoC

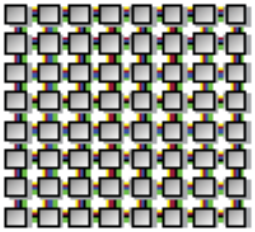
Challenge is trade-off network benefits of regular topology vs. heterogeneous, irregular Multicore SoC architectures



from INTEL

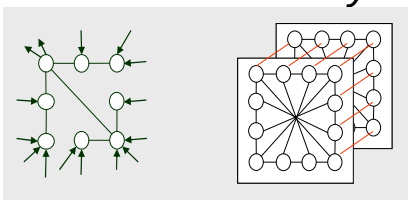
Spidergon STNoC family of topology

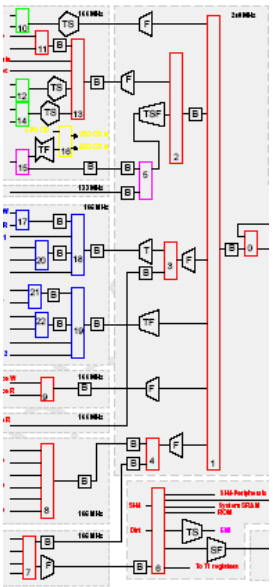




from TILERA

Spidergon STNoC hierarchy &

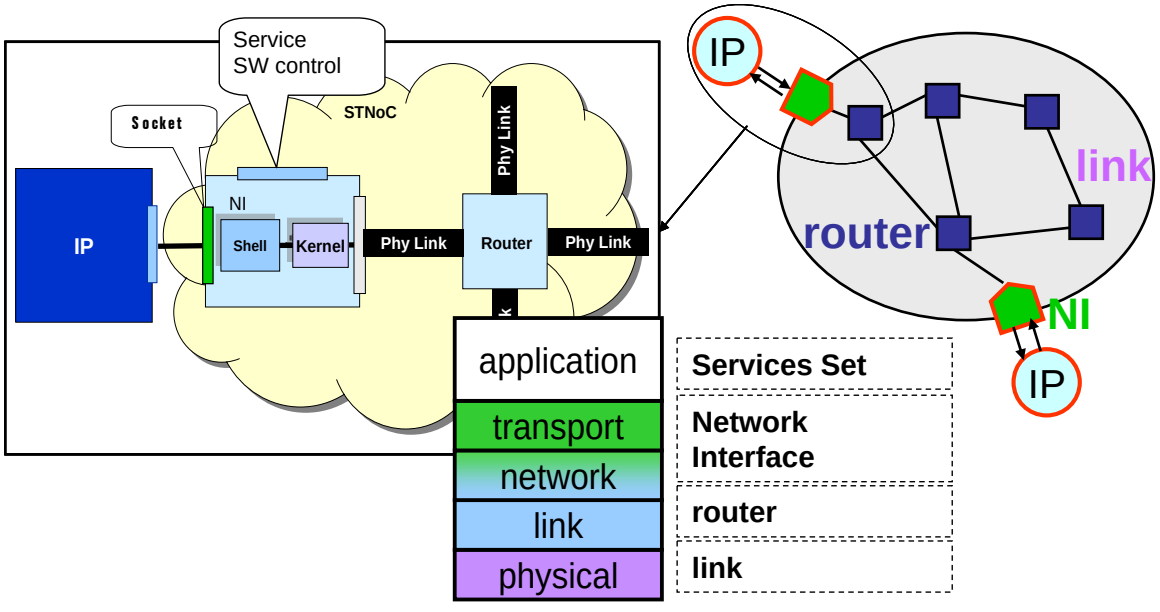




Example of STBus ICN

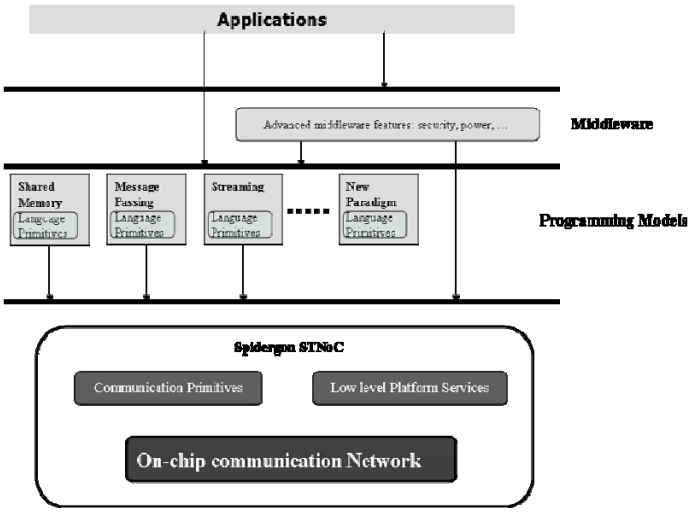
Spidergon STNoC on-chip communication platform

Spidergon STNoC is a set of **Services** on top of **Network Interfaces (NI)** (layer 4), **on-chip routers** (layers 3) and **physical links** (layer 1)



Spidergon STNoC: Software Stack

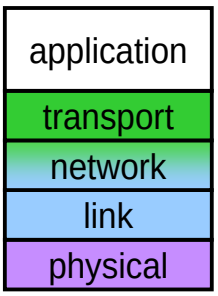
- Target: export an abstract view of the multi-core SoC architecture
- Libraries developed to ease programming and to take advantage of built-in NoC services
- A stack portable to different OS (but the API stays put) (e.g. Linux, Symbian)



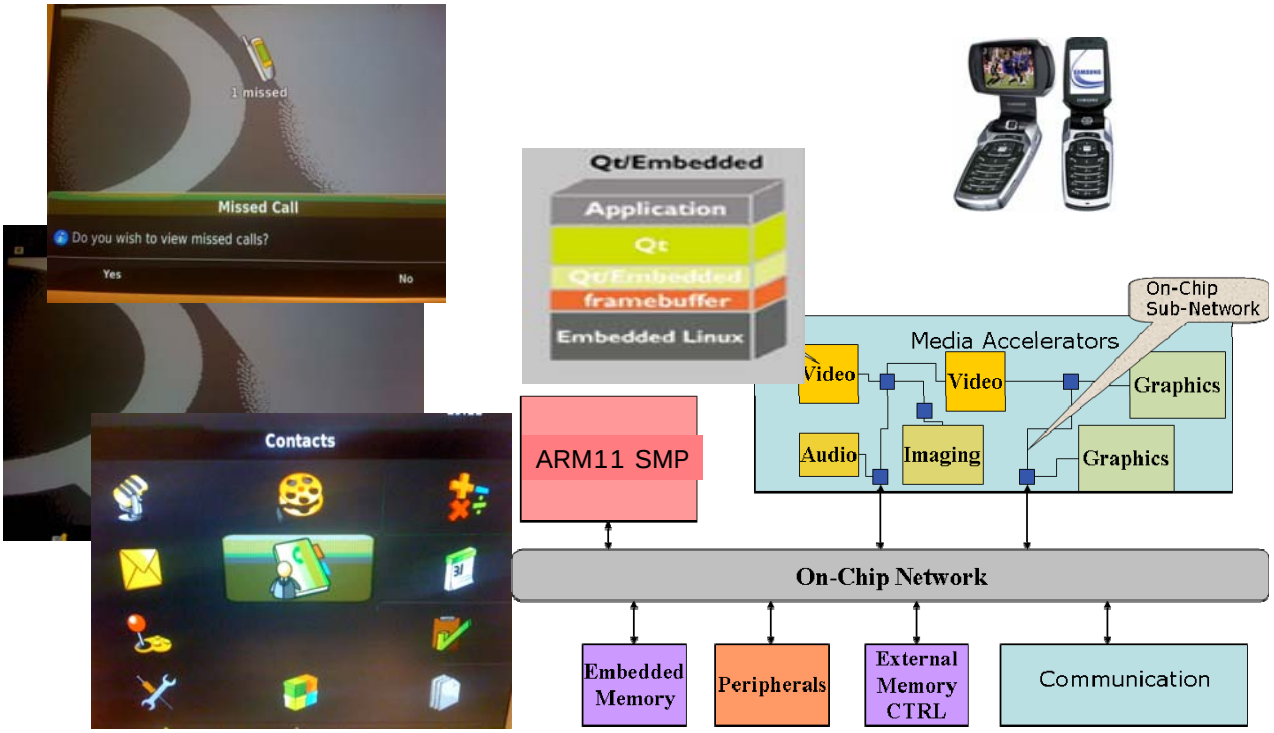
Spidergon STNoC: services

- Scratch your itch
  - A wealth of brand-new programming services
- Shared memory programming model
  - *load/store* communication primitives
  - Socket IP support: STBus, AXI protocols, OCP (on going)
- Message passing programming model
- Network awareness
  - Power management
  - Security
  - Quality of Service
  - fault tolerance

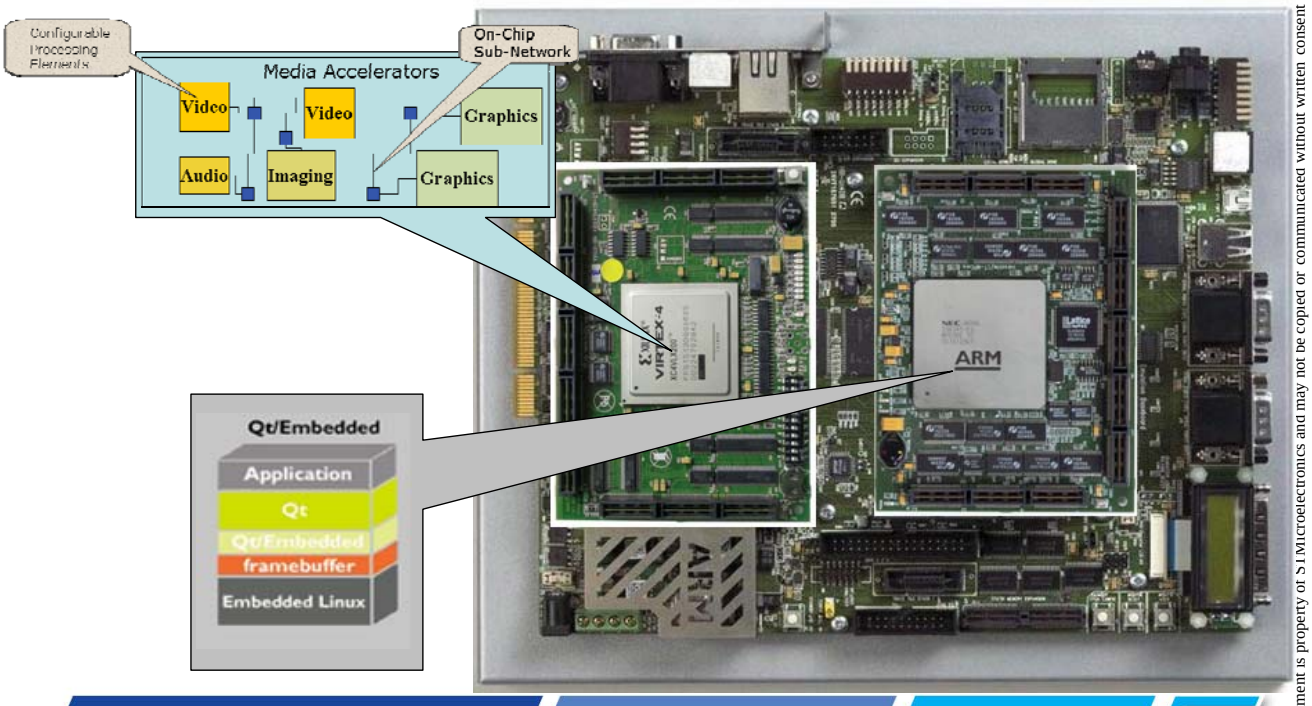
Enhanced user experience and Time to market



Emulate an application processor



Spidergon STNoC Multicore platform: ARM11 SMP based



Conclusions

- Spidergon STNoC is an innovative technology able to address the requirements of next generation multi-core SoCs

- For more info please refer to
  - Spidergon STNOC book
  - **ISBN:** 9781420044713
  - **Publication Date:** September 2008

- End of this year, we launch a Spidergon STNoC university program.
  - For more info please send me an email (Marcello.Coppola@st.com)